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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,643	11/15/2000	John E. Gavlik	P04762	3643

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EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,643	GAVLIK ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are subject to examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schurecht et al. (hereinafter Schurecht) (US 6, 260, 157) in view of Johnson et al. (hereinafter Johnson) (US 4,530,051)

Referring to claims 1 and 2,

Schurecht teaches an apparatus for controlling a physical layer interface of a network interface card in real time (Fig. 1, col. 3, line 66 through col. 4, line 14), said apparatus comprising:

a first memory capable of storing a multitasking control program, said multitasking control program comprising a main routine and a plurality of subroutines sequentially callable by said main routine (col. 4, line 43-45);

a second memory capable of storing a plurality of multitasking vectors associated with said multitasking control program (col. 4, line 61 –67) ; and

a microcontroller capable of executing said multitasking control program;

wherein program execution control is transferred from said main routine to a first one of said plurality of subroutines when said first subroutine is called by said main routine; and wherein the main routine, after sequentially transferring program execution control to each remaining subroutine in the plurality of subroutines, again transfers program execution control from the main routine to the first subroutine at the address of the decision point contained in the first multitasking vector, and the apparatus as set forth in Claim 1 wherein said main routine uses other multitasking vectors to subsequently and sequentially transfer program execution control back to each remaining subroutine at an address contained in each of the other multitasking vectors. (col. 4, line 45-67," 5) In conventional operation, the slave processor 30 retrieves program instructions or code from the program ROM 45 and executes the code instructions sequentially. As will be appreciated by those skilled in the art, code instructions may take various forms including jumps, calls, loads, etc. To enable patching of the program instructions within the ROM 45, one or more jump instructions are coded at convenient places within the ROM code. These jump instructions may, for example, be placed at every nth location within the code (where n is any integer), at the end or beginning of any subroutine, where jump instructions are already located within the code or at any other desired or logical location. Generally speaking, a patch may be performed at any or all of these jump instructions. Furthermore, to enable patching of the ROM code, a patch vector table is stored within the processing device 5 and is used by the jump instructions to identify where to jump or what patch program, if any, to implement at the jump

instruction. (6) The patch vector table may be stored in the external ROM 10 or the external RAM 15 and, if desired, may be transferred to the data RAM 65 of the ASIC 20 when patching is to be performed. However, the patch vector table may be stored at any other desired location within the processing device 5, such as in the program RAM 50, as long as the patch vector table is accessible by the slave processor 30."

Schurecht specifically fails to teach wherein said first subroutine, upon encountering a decision point in said first subroutine that is not yet capable of being decided, updates a first one of said plurality of multitasking vectors associated with said first subroutine with an address of said decision point and transfers program execution control back to said main routine; and Claim 1 wherein said main routine uses other multitasking vectors to subsequently and sequentially transfer program execution control back to each remaining subroutine at an address of a decision point contained in each of the other multitasking vectors.

Johnson teaches the process (main routine) comprising of a collection of procedures (a plurality of subroutines), each performing some subtask of the process. Johnson goes on teaching that the process for the needed data can call these procedures where the data is exchanged via stack (memory data structure) (col.4, lines 60-68 and col.5, lines 1-24). Johnson also teaches that the procedure can be placed into dormant state (a decision point that is not yet capable of being decided) and the status message of the procedure is updated (updating the vector of the subroutine) and then the process can resume another procedure by calling and transitioning to execution state. After the completion of another procedure, the process can come back

to the dormant procedure to continue the execution from where it left the procedure. (col. 7, lines 10-68 and col.8, lines 1-28, Figs.) and 5). Johnson also teaches in col. 6, lines 37-41, "Processes communicate with each other via interprocess messages which are placed in message queues such as message queue 240, which contains messages 241, 242, . . . , 243. These queues operate on a first-in, first-out queuing discipline in this example."

Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to combine the teachings of Johnson aiming to "A call message is sent to the remote processor and a remote process is initiated. When the selected procedure has been executed in the remote processor, a return message is sent to the home process and execution of the home process is continued." with the teachings of Schurecht such that a microcontroller within the system can manage multitasking control program by using other processors such as master processor through the mechanism taught by Schurecht wherein to permit execution of a process by two or more processors in a real time environment without substantial increase in system overhead as taught by Johnson.

Referring to claims 3, 4, 5 and 6,

Schurecht teaches the first memory as being a read-only memory (ROM), the second memory as being a random access memory, and both, ROM and RAM memories are internal to the microcontroller, and ROM as being an external device coupled to microcontroller through secondary bus. (Fig. 1, col.3, line 66 through col. 4, line 67).

Referring to claims 7 and 8,

Schurecht teaches the apparatus as set forth in Claim 2 wherein said first memory and said second memory comprise a random access memory (RAM) associated with said microcontroller, and the apparatus as set forth in Claim 7 wherein said RAM comprises an external device coupled to said microcontroller. (Fig. 1, col.3, line 66 through col. 4, line 67).

Referring to claims 9 and 10,

Claims 9 and 10 are rejected for the reasons set forth for the claims 1 and 2, and Cooper's teaching of a processing system including a data processor. (Fig. 1 element 104).

Referring to claims 11, 12, 13 and 14,

Claims 11, 12, 13 and 14 are rejected for the reasons set forth for the claims 3, 4, 5 and 6.

Referring to claims 15 and 16,

Claims 15 and 16 are rejected for the reasons set forth for the claims 7 and 8.

Referring to claims 17 and 18,

Claims 17 and 18 are the methods of the claims 1 and 2. Therefore claims 17 and 18 are rejected for the reasons set forth for claims 1 and 2.

Referring to claims 19, 20, 21 and 22,

Claims 19, 20, 21 and 22 are the methods of the claims 3, 4, 5 and 6. Therefore claims 19, 20, 21 and 22 are rejected for the reasons set forth for claims 3, 4, 5 and 6.

Referring to claim 23,

The apparatus of Claim 1, wherein the main routine repeatedly transfers program execution control to each of the plurality of subroutines, each time starting with the first subroutine and going sequentially through the remaining subroutines. (col. 4, line 45-67, col. 5, line 1-42)

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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JOHN FOLLANSBEE
PATENT EXAMINER
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